REMARKS

Claims 11-18 are pending in this application. For purposes of expedition, base claims 11, 12 and 14 have been amended in several particulars for purposes of clarity and brevity that are unrelated to patentability and prior art rejections while claims 17-18 have been newly added in accordance with current Office policy, to further and alternatively define Applicants' disclosed invention and to assist the Examiner to expedite compact prosecution of the instant application.

The title of the invention has been objected to for failing to be sufficiently descriptive. Accordingly, a new title of --SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND MANUFACTURING METHOD OF MINIATURIZATION OF MEMORY CELLS WITH REDUCED BIT LINES— is hereby submitted for the Examiner's consideration and entry.

Claims 11-16 have been rejected under 35 U.S.C. §112, first paragraph, because the specification and the drawings do not support the phrase "a diameter of said first opening is less than that of said second opening and such that said second opening reaches said semiconductor regions" as defined in base claims 11 and 14. Specifically, the Examiner suggests that the diameter of the first opening is larger than the second opening. In response thereto, base claims 11 and 14 have been carefully reviewed and amended to adopt the Examiner's suggestion by incorporating that "a diameter of [a] second opening is less than that of [a] first opening" in order to overcome the rejection.

More importantly, claims 11-16 have been rejected under 35 U.S.C. §102(e) as being anticipated by newly cited prior art, Kasai et al., U.S. Patent No. 6,448,597

for reasons stated on pages 3-6 of the Office Action (Paper No. 08062004). For purposes of expedition, base claims 11 and 14 have been amended to further clarify the structural relationship between the "first insulating film" and the "second insulating film", the "first opening" and the "second opening", and the "bit line" relative to the "first opening" and the "second insulating film" in order to clearly distinguish over Kasai '597.

For example, base claim 11, as amended, defines a semiconductor integrated circuit device, comprising:

> a semiconductor substrate with an active region defined by an element isolation region, word lines extending in a first direction over said active region such that gate electrodes of metal insulator semiconductor field effect transistors (MISFETs) are electrically coupled to said word lines, semiconductor regions formed in said active region extending in a second direction perpendicular to the first direction such that said semiconductor regions serve as a source region or a drain region of each MISFET;
> a first insulating film and a second insulating film covering said active region, said word lines and said semiconductor regions;
> a first opening formed in said first insulating film such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region;
> a second opening formed in said second insulating film under said first opening such that a diameter of said second opening in said first direction is less than that of said first opening, and such that said second opening reaches said semiconductor regions;
> a conductive material buried in said first opening and in said second opening; and
> a bit line formed on said first opening which is formed on said second insulating film such that said bit line is electrically coupled to said conductive material and extends to cross said word lines.

Likewise, base claim 14 defines a similar semiconductor integrated circuit device provided with an additional opening, i.e., "third opening formed in said first insulating film and said second insulating film to reach other semiconductor region."

As expressly defined in each of Applicants' base claims 11 and 14, novel

features of Applicants' claimed invention include: (1) an active region L which extends in a second direction perpendicular to the first direction, as shown, for example, in FIG. 31; (2) a second insulating film 11 which is formed under the first insulating film 46, as shown, for example, in FIG. 36; (3) a second opening which is formed in said second insulating film 11 under said first opening such that a diameter of said second opening in the first direction is less than that of said first opening and such that said second opening reaches semiconductor regions 8, as shown, for example, in FIG. 36; and (4) a bit line BL which is formed on the first opening which is, in turn, formed on the second insulating film 11. This arrangement advantageously enables the bit line BL and the semiconductor regions 8 to be connected without having either to partially fatten the width of bit line and extend up to the location overlying the active region or to fold part of the active region in the direction of the bit lines, as described on page 23, lines 11-17 of Applicants' specification.

In contrast to Applicants' base claims 11 and 14, Kasai '597 discloses a DRAM having a stacked capacitor in each memory cell. As shown in FIGs. 8-10, the DRAM includes memory cells each including a MOSFET having a gate electrode and a pair of diffused regions 36, a stacked capacitor 52 having a bottom electrode 56 of a cylindrical shape, a top electrode 62, at least a portion of the top electrode 62 being received in the bottom electrode 56, and a capacitor dielectric film 60 sandwiched between the top electrode 62 and the bottom electrode 56, and a capacitor contact 18 for connecting one of the diffused regions 36 to the bottom electrode 56.

However, Kasai '597 does **not** disclose or suggest how to connect the bit line 38 and the diffused region 36, as shown in FIG. 1 and FIG. 2 of Applicants' disclosure and, certainly, does **not** disclose how to shape the opening of the connection between the bit line 38 and the diffused region 36. More importantly, Kasai '597 does not disclose or suggest Applicants' claimed "first opening formed in said first insulating film such that said first opening is arranged between said word lines and extends, in said first direction, from a semiconductor region to said element isolation region"; "second opening formed in said second insulating film under said first opening such that a diameter of said second opening in said first direction is less than that of said first opening, and such that said second opening reaches said semiconductor regions" and "bit line formed on said first opening which is formed on said second insulating film such that said bit line is electrically coupled to said conductive material and extends to cross said word lines" as expressly defined in Applicants' base claims 11 and 14.

The rule under 35 U.S.C. §102 is well settled that anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. In re Paulsen, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Those elements must either be inherent or disclosed expressly and must be arranged as in the claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); Verdegall Bros., Inc. v. Union Oil Co., 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). The corollary of that rule is that absence from the reference of

any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986).

The burden of establishing a basis for denying patentability of a claimed invention rests upon the Examiner. The limitations required by the claims cannot be ignored. See In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). All claim limitations, including those which are functional, must be considered. See In re Oelrich, 666 F.2d 578, 212 USPQ 323 (CCPA 1981). Hence, all words in a claim must be considered in deciding the patentability of that claim against the prior art. Each word in a claim must be given its proper meaning, as construed by a person skilled in the art. Where required to determine the scope of a recited term, the disclosure may be used. See In re Barr, 444 F.2d 588, 170 USPQ 330 (CCPA 1971).

In the present situation, Kasai '597 fails to disclose and suggest key features of Applicants' base claims 11 and 14. Therefore, Applicants respectfully request that the rejection of claims 11-16 be withdrawn.

Claims 17-18 have been newly added to alternatively define Applicants' disclosed invention over the prior art of record. These claims are believed to be allowable at least for the same reasons discussed against all the outstanding rejections of the instant application. No fee is incurred by the addition of claims 17-18.

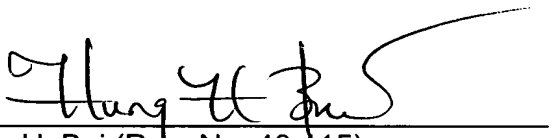
In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is

requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, No. 01-2135 (Application No. 501.37959CC2), and please credit any excess fees to said deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By 

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